UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,565	10/31/2005	Edward Fuergut	I431.126.101/FIN 481 PCT/	9154

25281 7590 10/02/2006

DICKE, BILLIG & CZAJA, P.L.L.C.
FIFTH STREET TOWERS
100 SOUTH FIFTH STREET, SUITE 2250
MINNEAPOLIS, MN 55402

EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/529,565	FUERGUT ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/01/06*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 10-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 10, 11,15, 19 and 21, the "active upper face" of the first semiconductor chip does not describe the face pointing upwards as illustrated in the figures, and is downwards facing. The "upper face areas of a plastic encapsulation compound" recited in claim 10, along with the "upper face" of the first chip, form an "overall upper face" which again faces downwards (towards the outer contact pads) in the illustrations. The claims have been interpreted in light of the drawings to mean that the "upper face" is the outward active face of the flip-chip mounted of the first semiconductor chip, and the "overall upper face" is the outer contact area of the component. Regarding claim 15, "upper faces" of the contact pillars lacks antecedent basis, and also describes a portion of the pillars which points downwards in the illustrations.

Claim Objections

3. Claim 13 is objected to because of the following informalities: the claim depends from claim 1 instead of claim 10. Appropriate correction is required.

4. Claim 20 is objected to because of the following informalities: "float connectors" lacks proper antecedent basis, and is interpreted to mean "flat conductors". Appropriate correction is required.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **10-25** are rejected under 35 U.S.C. 102(e) as being anticipated by Hoffman (6,737,750).

6. Regarding claim **10** as best understood, Hoffman discloses in Fig 6A an electronic component comprising: a stack of semiconductor chips having a first semiconductor chip (12) and a stacked second semiconductor chip (16), the semiconductor chips having an *active upper face* with contact pads to integrated circuits and a rear face; a flat conductor structure (14) having a chip island (14i), flat conductors (horizontal portions of 14k) surrounding the chip island, and contact pillars (vertical portions of 14k) arranged on the flat conductors and aligned orthogonally with respect to the flat conductors; wherein the second semiconductor chip (16) is arranged with its rear face (16b) on the chip island and wherein its contact pads (16c) are electrically connected via bonding wire connections (20) to the flat conductors; wherein the first semiconductor chip (12) is surrounded by the contact pillars (vertical portions of 14k) and is arranged underneath the chip island (14i) such that pillar contact pads (14m) of the contact

pillars, *upper face areas* of a plastic encapsulation compound that embeds the semiconductor chips, the contact pillars and the flat conductor structure, and the *active upper face* (can be connected in a flip-chip manner, col 4 ln 26-30) of the first semiconductor chip, form an *overall upper face* (10a), and wherein a wiring layer (11a) is arranged on the overall upper face and electrically connects the semiconductor chips to one another via wiring lines.

7. With regards to claims **11 and 12** as best understood, Hoffman discloses in Fig 6A the component of claim 10, wherein the wiring layer (11a) comprises a wiring level (10) arranged on *the overall upper face* (10a) and comprises outer contact pads (11b) that are electrically connected via the wiring lines (11a) to the pillar contact pads (14m) of the contact pillars (vertical portions of 14k), and wherein solder balls (15) are arranged on the outer contact pads (11b).

8. With regards to claims **13 and 14** as best understood, Hoffman discloses in Fig 15 the component of *claim 10* configured within a panel comprising a leadframe with additional electronic components arranged in rows and columns (col 12 ln 1-5) wherein the shape of the panel corresponds in its extent and extent markings to a standard semiconductor wafer (col 13 ln 8-15).

9. Regarding claim **15**, as best understood Hoffman discloses in Fig 15 a method for production of a panel for a plurality of electronic components comprising: producing leadframe with component positions arranged in rows and columns (col 12 ln 1-5), whereby a component position comprises a chip island and flat conductors which surround the chip island (see Fig 6A), as well as

contact pillars, which are arranged on the flat conductors and are aligned orthogonally with respect to the flat conductors; applying a stacked semiconductor chip to the chip island of the component positions (steps 3-5 of Fig 15); producing bonding wire connections (step 6) between the flat conductors and contact pads on *active upper faces* of the stacked semiconductor chips; applying first semiconductor chips with their active upper faces to a carrier with adhesive bonding on one side (step 2, col 7 ln 22-24), with the first semiconductor chips being arranged in rows and columns which correspond to the rows and columns of the component positions; applying the leadframe with stacked semiconductor chips to the carrier (step 4) in such a way that the contact pillars of the leadframe are adhesively bonded by *their upper faces* to the carrier and the first semiconductor chips are arranged on the carrier underneath the chip islands of the leadframe and are surrounded by contact pillars (see Fig 6A); embedding the leadframe with stacked semiconductor chips and bonding wire connections in a plastic compound (Fig 6A item 19) to form a composite body on the carrier (step 7); removing the carrier (col 12 ln 9-11) exposing an overall upper face composed of active upper faces of the first semiconductor chips, pillar contact pads of the contact pillars, and an upper face of the plastic compound; applying a wiring layer (10) to *the overall upper face*, forming wiring lines and outer contact pads; and wherein the wiring lines connect the outer contact pads to the contact pads of the first semiconductor chip (see Fig 6A).

10. Regarding claim **16**, Hoffman discloses the method of claim 15 further comprising applying solder balls to the outer contact pads to provide outer contacts (Fig 15 step 8).

11. Regarding claim **17**, Hoffman discloses the method of claim 15 further comprising separating the panel into individual electronic components (Fig 15 step 9).

12. Regarding claim **18**, Hoffman discloses the method of claim 17, further comprising applying outer contact pads of an electronic component (see Fig 6A item 11b).

13. With regards to claims **19-21** as best understood, Hoffman discloses in Fig 6A an electronic component comprising: a first semiconductor chip (12) having an *active upper face* (can be connected in a flip-chip manner, col 4 ln 26-30), contact pads (12c), and a rear face (12b); a stacked second conductor chip (16) having an active upper face (16a), contact pads (16c) and a rear face (16b); a chip island (14i); flat conductors (horizontal portions of 14k) surrounding the chip island; contact pillars (vertical portions of 14k) arranged on the flat conductors and surrounding the first semiconductor chip; wherein the second semiconductor chip is arranged with its rear face on the chip island; bonding wire means (20) for electrically connecting the contact pads of the second semiconductor chip to the flat connectors; a plastic encapsulation compound (19) configured to embed the first and second semiconductor chips, the contact pillars, the chip island, and the flat conductors; wherein the first semiconductor chip (12) is arranged under the

chip island such that pillar contact pads of the contact pillars, upper face areas of the plastic encapsulation compound, and *the active upper face* of the first semiconductor chip form an *overall upper face* (10a); and a wiring layer (11a) on the *overall upper face* for electrically connecting the first and second semiconductor chips to each other via (col 7 ln 14-15 and col 10 ln 8-10).

14. With regards to claims **22 and 23** as best understood, Hoffman discloses in Fig 6A the component of claim 10, wherein the wiring layer (11a) comprises a wiring level (10) arranged on *the overall upper face* (10a) and comprises outer contact pads (11b) that are electrically connected via the wiring lines (11a) to the pillar contact pads (14m) of the contact pillars (vertical portions of 14k), and wherein solder balls (15) are arranged on the outer contact pads (11b).

15. With regards to claims **24 and 25** as best understood, Hoffman discloses in Fig 15 the component of *claim 10* configured within a panel comprising a leadframe with additional electronic components arranged in rows and columns (col 12 ln 1-5) wherein the shape of the panel corresponds in its extent and extent markings to a standard semiconductor wafer (col 13 ln 8-15).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John C Ingham
Examiner
Art Unit 2814

jci

HOWARD WEISS
PRIMARY EXAMINER